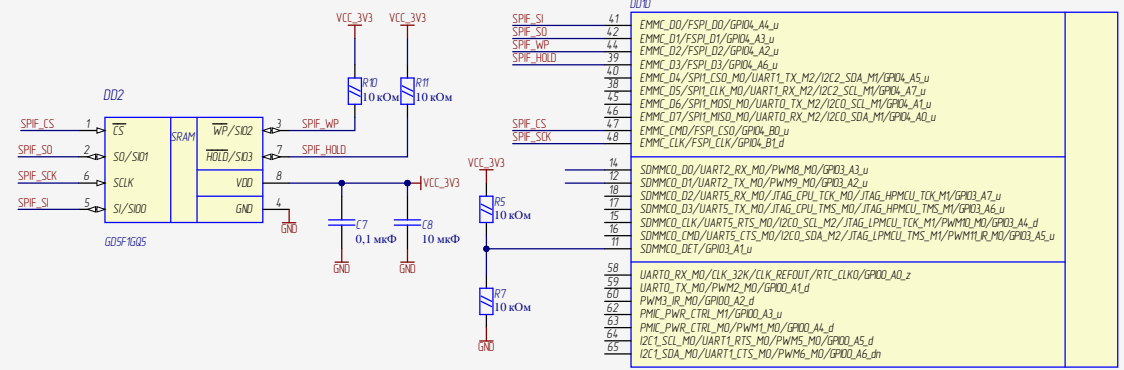
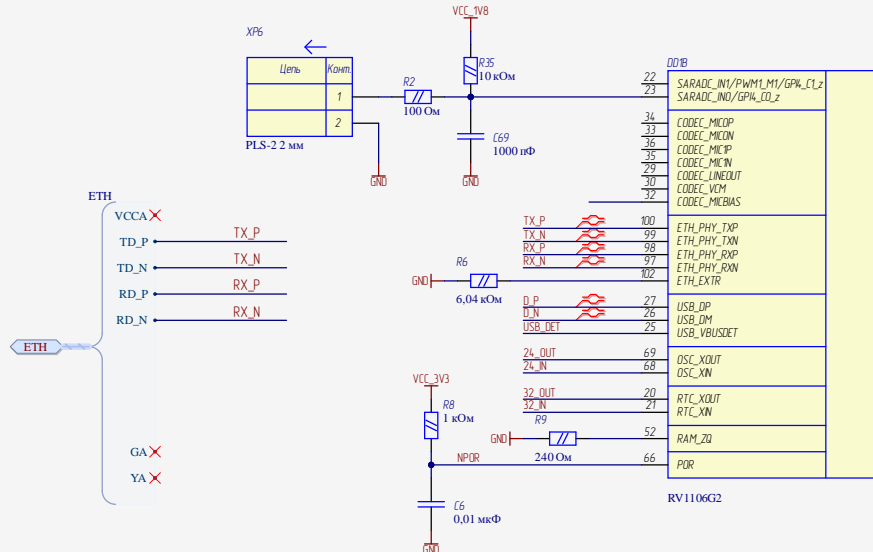
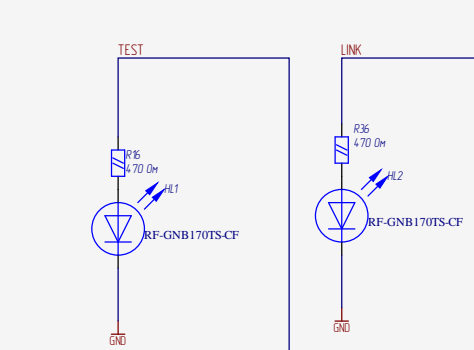
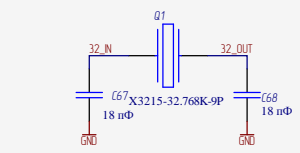
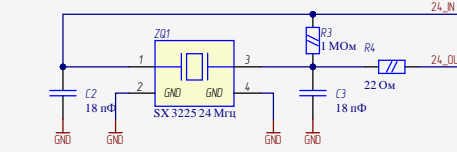


				A8.240.05 ЭЗ			
				Плата управления			
Изм.	Лист	№ докум.	Подп.	Дата	Лит.	Масса	Масштаб
		Панькин			01		1:1
Разраб.		Кацулин					
Проб.							
Т.контр.		Андреев					
Н.контр.		Жданова					
Утв.		Кузьминский					
					Лист 1	Листов 3	
					000 "ЭЛК"		

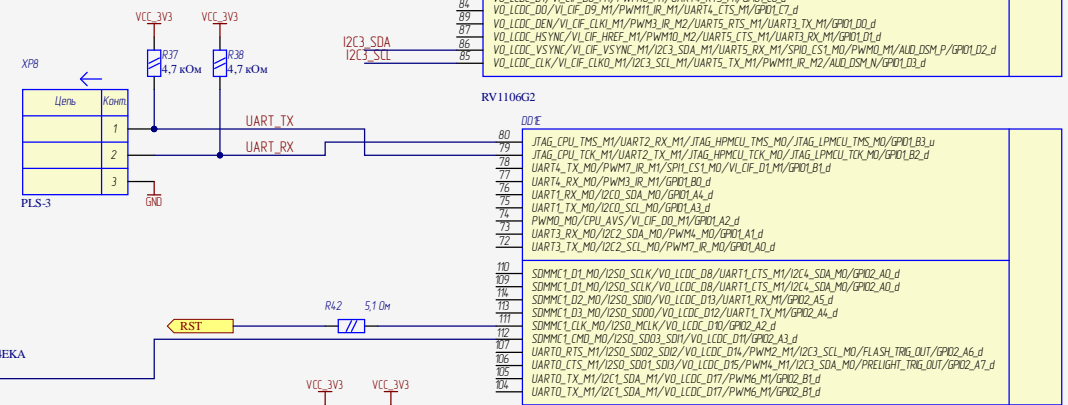
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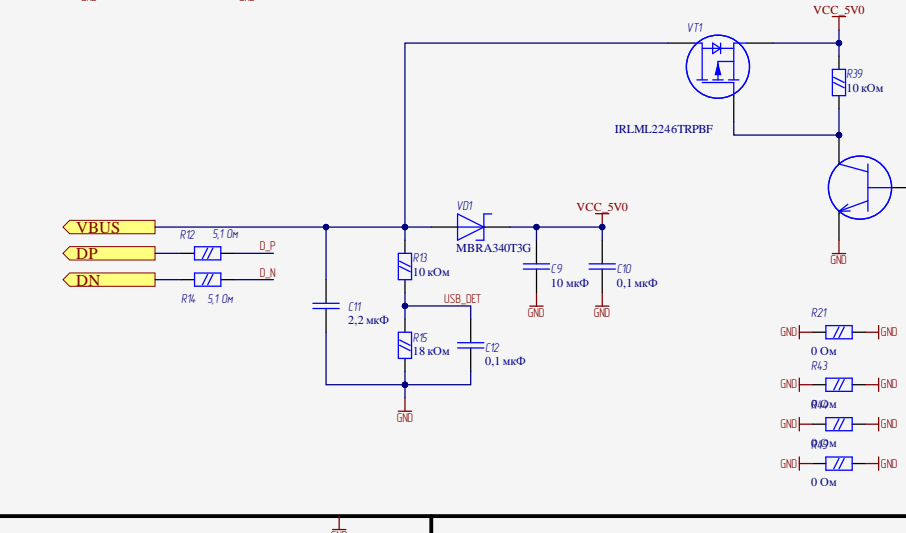
SPIF_SI	41	EMMC_D0/FSP_LD0/GPI0_A4_u
SPIF_S0	42	EMMC_D1/FSP_LD1/GPI0_A3_u
SPIF_WP	44	EMMC_D2/FSP_LD2/GPI0_A2_u
SPIF_HOLD	39	EMMC_D3/FSP_LD3/GPI0_A6_u
	40	EMMC_D4/SPI_CS0_M0/UART1_TX_M2/I2C2_SDA_M1/GPI0_A5_u
	38	EMMC_D5/SPI_CLK_M0/UART1_RX_M2/I2C2_SCL_M1/GPI0_A7_u
	45	EMMC_D6/SPI_M0SL_M0/UART0_TX_M2/I2C0_SCL_M1/GPI0_A1_u
	46	EMMC_D7/SPI_M0SD_M0/UART0_RX_M2/I2C0_SDA_M1/GPI0_A0_u
SPIF_CS	37	EMMC_CMD/FSP_CS0/GPI0_B0_u
SPIF_STK	48	EMMC_CLK/FSP_CLK/GPI0_B1_d
	14	SDMMC0_D0/UART2_RX_M0/PWM8_M0/GPI0_A3_u
	12	SDMMC0_D1/UART2_TX_M0/PWM9_M0/GPI0_A2_u
	18	SDMMC0_D2/UART5_RX_M0/JTAG_CPU_TCK_M0/JTAG_HPMCUL_TCK_M1/GPI0_A7_u
	17	SDMMC0_D3/UART5_TX_M0/JTAG_CPU_TMS_M0/JTAG_HPMCUL_TMS_M1/GPI0_A6_u
	15	SDMMC0_CLK/UART5_RTS_M0/I2C0_SCL_M2/JTAG_LPMCUL_TCK_M1/PWM10_M0/GPI0_A4_d
	16	SDMMC0_CMD/UART5_CTS_M0/I2C0_SDA_M2/JTAG_LPMCUL_TMS_M1/PWM10_M0/GPI0_A5_u
	11	SDMMC0_DET/GPI0_A1_u
	58	UART0_RX_M0/CLK_32K/CLK_REFOUT/RTC_CLK/GPI0_A0_z
	59	UART0_TX_M0/PWM2_M0/GPI0_A1_d
	60	PWM3_IR_M0/GPI0_A3_u
	62	PWM3_CTRL_M0/GPI0_A4_d
	63	PWM3_PWR_CTRL_M0/PWM1_M0/GPI0_A4_d
	64	I2C1_SCL_M0/UART1_RTS_M0/PWM5_M0/GPI0_A5_d
	65	I2C1_SDA_M0/UART1_CTS_M0/PWM6_M0/GPI0_A6_dh

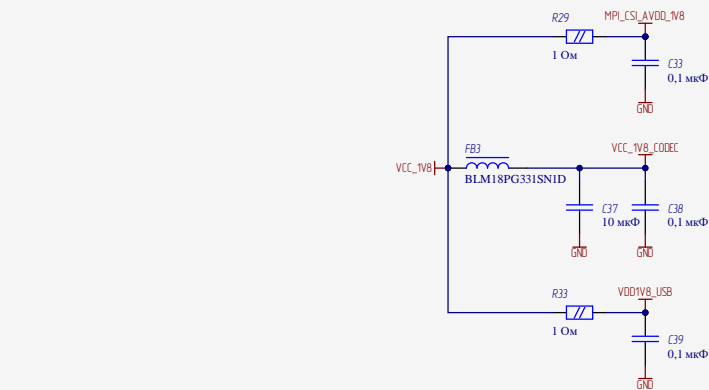
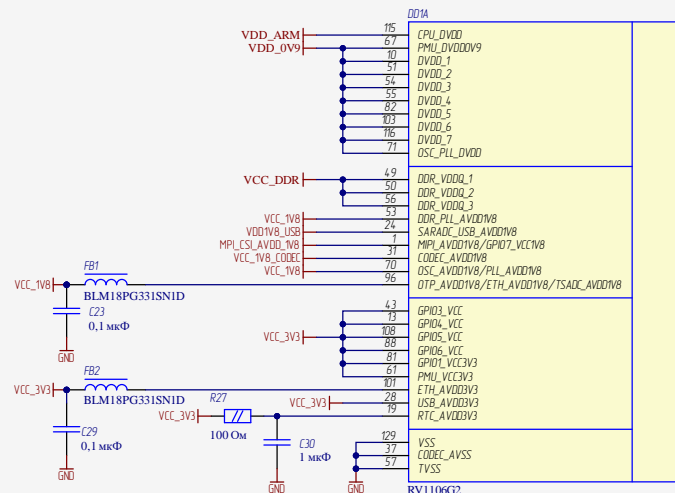
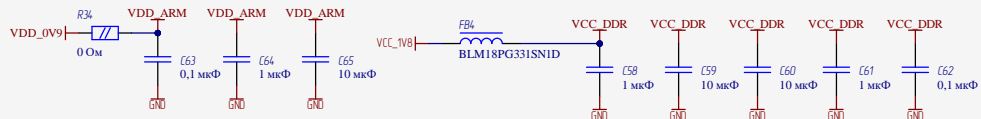
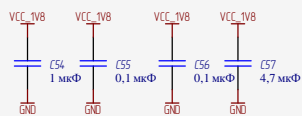
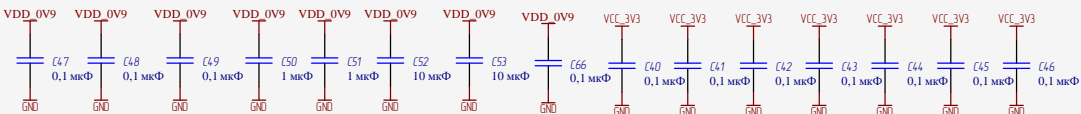
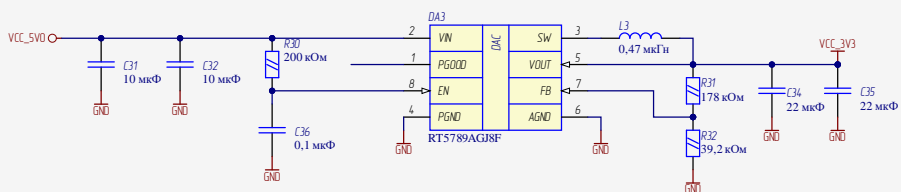
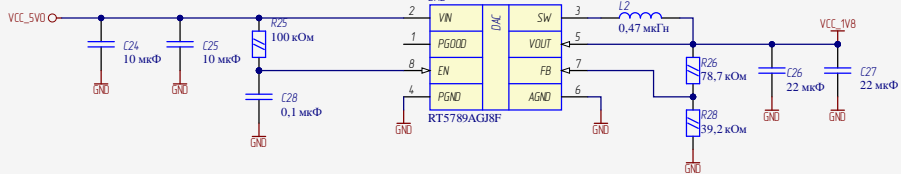
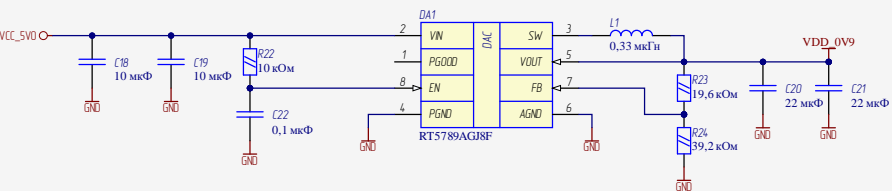
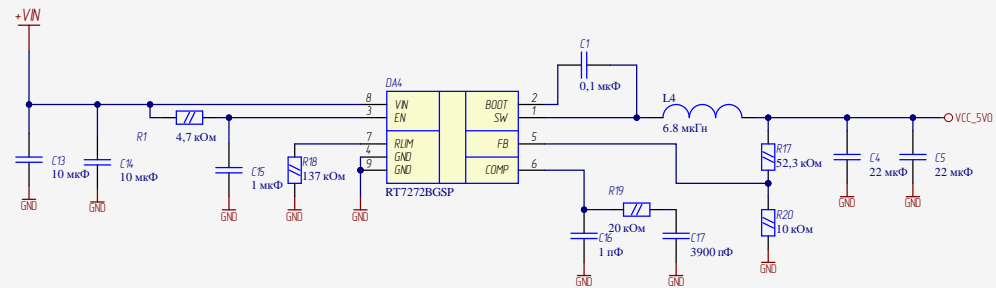


DD1C	2	VL_CIF_CLK0_M0/MPI_CLK0_OUT/GPI0_C4_d	
	3 <th>4</th> <td>VL_CIF_VSYN0_M0/GPI0_C5_d</td>	4	VL_CIF_VSYN0_M0/GPI0_C5_d
	4 <td>VL_CIF_D10/PWM7_IR_M2/MPI_CLK1_OUT/GPI0_C6_d</td>	VL_CIF_D10/PWM7_IR_M2/MPI_CLK1_OUT/GPI0_C6_d	
	5 <td>VL_CIF_D11/UART5_TX_M2/I2C4_SCL_M2/GPI0_C7_d</td>	VL_CIF_D11/UART5_TX_M2/I2C4_SCL_M2/GPI0_C7_d	
	6 <td>VL_CIF_D13/UART5_RTS_M2/I2C3_SCL_M2/GPI0_D1_d</td>	VL_CIF_D13/UART5_RTS_M2/I2C3_SCL_M2/GPI0_D1_d	
	7 <td>VL_CIF_D12/UART5_RX_M2/I2C4_SDA_M2/GPI0_D0_d</td>	VL_CIF_D12/UART5_RX_M2/I2C4_SDA_M2/GPI0_D0_d	
	8 <td>VL_CIF_D14/UART5_CTS_M2/I2C3_SDA_M2/GPI0_D2_d</td>	VL_CIF_D14/UART5_CTS_M2/I2C3_SDA_M2/GPI0_D2_d	
	9 <td>VL_CIF_D15/PWM1_M2/GPI0_D3_d</td>	VL_CIF_D15/PWM1_M2/GPI0_D3_d	
	128 <td>VL_CIF_HREF_M0/MPI_CSI_RX_D0P/LVDS_RX_D0P/GPI0_C3_d</td>	VL_CIF_HREF_M0/MPI_CSI_RX_D0P/LVDS_RX_D0P/GPI0_C3_d	
	127 <td>VL_CIF_CLK1_M0/MPI_CSI_RX_D0N/LVDS_RX_D0N/GPI0_C2_d</td>	VL_CIF_CLK1_M0/MPI_CSI_RX_D0N/LVDS_RX_D0N/GPI0_C2_d	
	126 <td>VL_CIF_D9_M0/MPI_CSI_RX_CK0P/LVDS_RX_CK0P/GPI0_C1_d</td>	VL_CIF_D9_M0/MPI_CSI_RX_CK0P/LVDS_RX_CK0P/GPI0_C1_d	
	125 <td>VL_CIF_D8_M0/MPI_CSI_RX_CK0N/LVDS_RX_CK0N/GPI0_C0_d</td>	VL_CIF_D8_M0/MPI_CSI_RX_CK0N/LVDS_RX_CK0N/GPI0_C0_d	
	123 <td>VL_CIF_D7_M0/MPI_CSI_RX_D1P/LVDS_RX_D1P/GPI0_B7_d</td>	VL_CIF_D7_M0/MPI_CSI_RX_D1P/LVDS_RX_D1P/GPI0_B7_d	
	122 <td>VL_CIF_D6_M0/MPI_CSI_RX_D1N/LVDS_RX_D1N/GPI0_B6_d</td>	VL_CIF_D6_M0/MPI_CSI_RX_D1N/LVDS_RX_D1N/GPI0_B6_d	
	121 <td>VL_CIF_D5_M0/MPI_CSI_RX_D2P/LVDS_RX_D2P/GPI0_B5_d</td>	VL_CIF_D5_M0/MPI_CSI_RX_D2P/LVDS_RX_D2P/GPI0_B5_d	
	121 <td>VL_CIF_D4_M0/MPI_CSI_RX_D2N/LVDS_RX_D2N/GPI0_B4_d</td>	VL_CIF_D4_M0/MPI_CSI_RX_D2N/LVDS_RX_D2N/GPI0_B4_d	
	120 <td>VL_CIF_D3_M0/MPI_CSI_RX_CK1P/LVDS_RX_CK1P/GPI0_B3_d</td>	VL_CIF_D3_M0/MPI_CSI_RX_CK1P/LVDS_RX_CK1P/GPI0_B3_d	
	119 <td>VL_CIF_D2_M0/MPI_CSI_RX_CK1N/LVDS_RX_CK1N/GPI0_B2_d</td>	VL_CIF_D2_M0/MPI_CSI_RX_CK1N/LVDS_RX_CK1N/GPI0_B2_d	
	118 <td>VL_CIF_D1_M0/MPI_CSI_RX_D3P/LVDS_RX_D3P/GPI0_B1_d</td>	VL_CIF_D1_M0/MPI_CSI_RX_D3P/LVDS_RX_D3P/GPI0_B1_d	
	117 <td>VL_CIF_D0_M0/MPI_CSI_RX_D3N/LVDS_RX_D3N/GPI0_B0_d</td>	VL_CIF_D0_M0/MPI_CSI_RX_D3N/LVDS_RX_D3N/GPI0_B0_d	
	95 <td>VO_LCDC_D7/VL_CIF_D2_M1/PWM2_M2/SPI0_CS0_M0/SDMMC1_D1_M1/GPI0_C0_d</td>	VO_LCDC_D7/VL_CIF_D2_M1/PWM2_M2/SPI0_CS0_M0/SDMMC1_D1_M1/GPI0_C0_d	
	94 <td>VO_LCDC_D6/VL_CIF_D3_M1/PWM4_M2/SPI0_CLK_M0/SDMMC1_D0_M1/GPI0_C1_d</td>	VO_LCDC_D6/VL_CIF_D3_M1/PWM4_M2/SPI0_CLK_M0/SDMMC1_D0_M1/GPI0_C1_d	
	93 <td>VO_LCDC_D5/VL_CIF_D4_M1/PWM5_M2/I2C4_SCL_M1/SDMMC1_M0/SPI0_C1_M0/GPI0_C2_d</td>	VO_LCDC_D5/VL_CIF_D4_M1/PWM5_M2/I2C4_SCL_M1/SDMMC1_M0/SPI0_C1_M0/GPI0_C2_d	
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	91 <td>VO_LCDC_D3/VL_CIF_D6_M1/PWM8_M1/UART4_RX_M1/SDMMC1_D3_M1/GPI0_C4_d</td>	VO_LCDC_D3/VL_CIF_D6_M1/PWM8_M1/UART4_RX_M1/SDMMC1_D3_M1/GPI0_C4_d	
	90 <td>VO_LCDC_D2/VL_CIF_D7_M1/PWM9_M1/UART4_TX_M1/SDMMC1_D2_M1/GPI0_C5_d</td>	VO_LCDC_D2/VL_CIF_D7_M1/PWM9_M1/UART4_TX_M1/SDMMC1_D2_M1/GPI0_C5_d	
	83 <td>VO_LCDC_D1/VL_CIF_D8_M1/PWM10_M1/UART4_RTS_M1/GPI0_C6_d</td>	VO_LCDC_D1/VL_CIF_D8_M1/PWM10_M1/UART4_RTS_M1/GPI0_C6_d	
	84 <td>VO_LCDC_D0/VL_CIF_D9_M1/PWM11_M1/UART4_CTS_M1/GPI0_C7_d</td>	VO_LCDC_D0/VL_CIF_D9_M1/PWM11_M1/UART4_CTS_M1/GPI0_C7_d	
	89 <td>VO_LCDC_DEN/VL_CIF_CLK1_M1/PWM3_IR_M2/UART5_RTS_M1/UART3_TX_M1/GPI0_D0_d</td>	VO_LCDC_DEN/VL_CIF_CLK1_M1/PWM3_IR_M2/UART5_RTS_M1/UART3_TX_M1/GPI0_D0_d	
	87 <td>VO_LCDC_HSYN0/VL_CIF_HREF_M1/PWM10_M2/UART5_CTS_M1/UART3_RX_M1/GPI0_D1_d</td>	VO_LCDC_HSYN0/VL_CIF_HREF_M1/PWM10_M2/UART5_CTS_M1/UART3_RX_M1/GPI0_D1_d	
	86 <td>VO_LCDC_VSYN0/VL_CIF_VSYN0_M1/I2C3_SDA_M1/UART5_RTS_M1/SPI0_CS1_M0/PWM10_M1/AUD_DSM_P/GPI0_D2_d</td>	VO_LCDC_VSYN0/VL_CIF_VSYN0_M1/I2C3_SDA_M1/UART5_RTS_M1/SPI0_CS1_M0/PWM10_M1/AUD_DSM_P/GPI0_D2_d	
	85 <td>VO_LCDC_CLK0/VL_CIF_CLK0_M0/I2C3_SCL_M1/UART5_TX_M1/PWM11_IR_M2/AUD_DSM_P/GPI0_D3_d</td>	VO_LCDC_CLK0/VL_CIF_CLK0_M0/I2C3_SCL_M1/UART5_TX_M1/PWM11_IR_M2/AUD_DSM_P/GPI0_D3_d	



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B

A

A

Инд. № докум.

Взам. инд. №

Подл. и дата

Инд. № подл.